29C310

T1 CSU / ISDN PRI Transceiver

Description

The 29C310 is the first fully integrated transceiver for T1 CSU and ISDN Primary Rate Interface (ISDN PRI) applications at 1.544 MHz. This transceiver operates over 6,000 feet of 22 AWG twisted-pair cable without any external components. To compensate for shorter lines, 7.5 dB, and 22.5 dB frequency-dependent transmit Line Build-Outs (LBOs) are provided.

The device offers selectable B8ZS encoding/decoding, and unipolar or bipolar data I/O. It also provides jitter attenuation in either the transmit or receive direction starting at 3 Hz, and incorporates a serial interface (SIO) for microprocessor control.

The 29C310 offers a variety of diagnostic features including loopbacks and loss of signal monitoring. It uses an advanced double-poly, double-metal CMOS process and requires only a single 5-volt power supply.

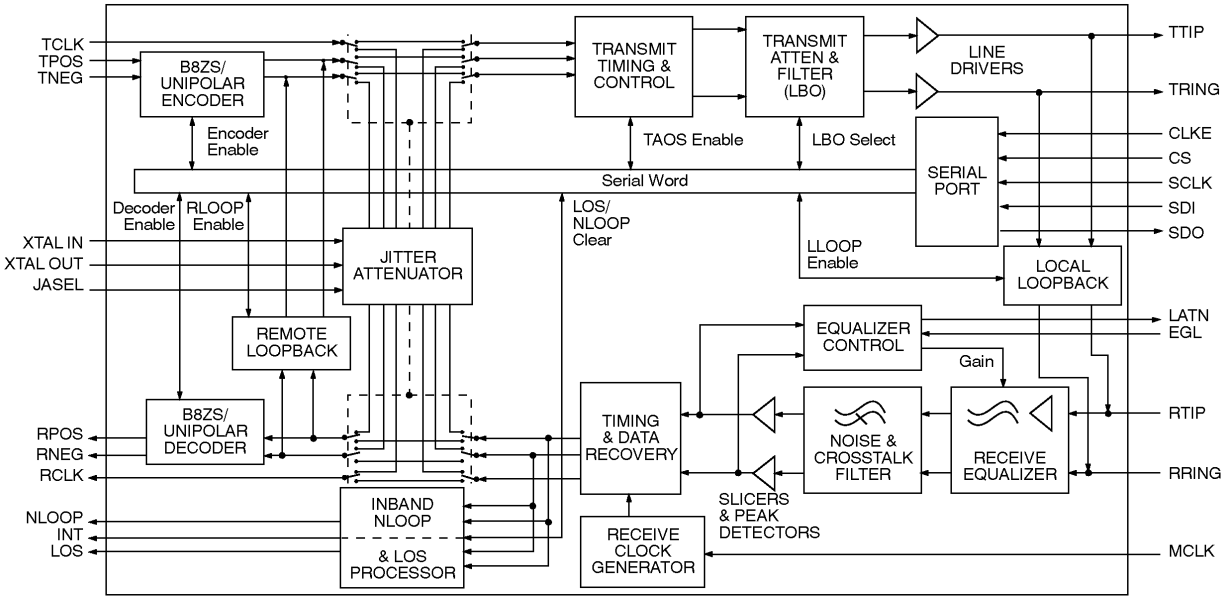
The MHS 29C310 finds applications in widely diverse areas of telecommunication, including

- ISDN Primary Rate Interface (PRI) (ANSI T1.408)
- CSU interface to T1 Service (Pub 62411)
- DS1 Metallic Interface (ANSI T1.403)
- T1 LAN bridge
- CPU to CPU Channel Extenders
- Digital Loop Carrier – Subscriber Carrier Systems
- T1 Mux
- Channel Banks

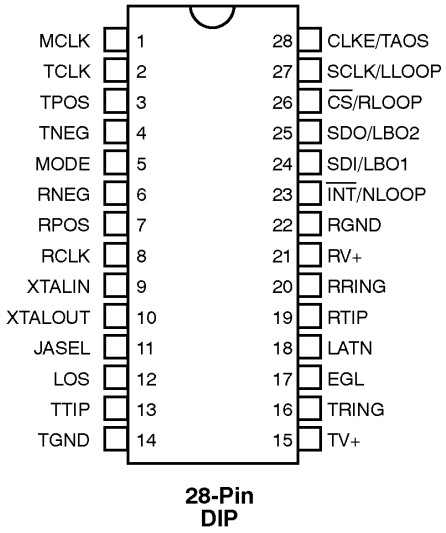
Features

- Fully integrated transceiver comprising : on-chip equalizer ; timing recovery/control ; data processor ; receiver ; and transmitter with line build-out and digital control
- Meets or exceeds ANSI and CCITT specifications including T1.403, T1.408, and AT&T PUB 62411
- Selectable receiver sensitivity. Fully restores the received signal after transmission through a cable with attenuation of either 0 to 26 dB, or to 36 dB @772 KHz
- Selectable unipolar or bipolar data I/O
- Selectable B8ZS encoding/decoding
- Line attenuation indication output
- 138 UI jitter tolerance at 1 Hz
- Output short circuit current limit protection
- On-line idle mode for redundant systems
- 7.5 dB, 15 dB, and 22.5 dB transmit LBOS
- Local, remote and inband network loopback functions
- Receive monitor with loss of signal (LOS) output
- Jitter attenuation starting at 3 Hz, switchable to transmit or receive path
- Microprocessor controllable

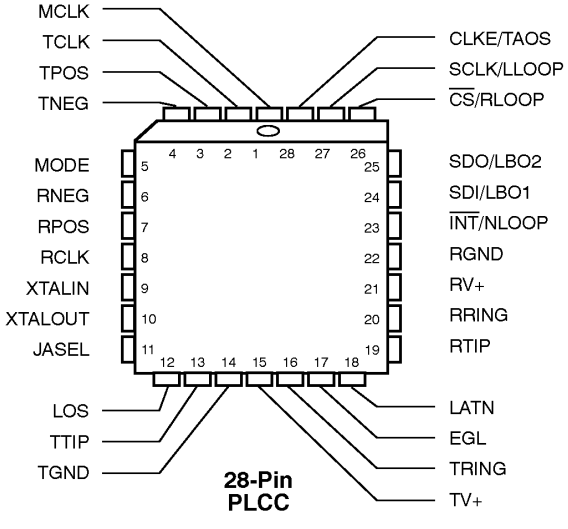
Figure 1. 29C310 Block Diagram



Interface



28-Pin DIP



28-Pin PLCC

Table 1 : Pin Description

Symbol	Pin #	I/O	Name	Description
MCLK	1	I	Master Clock	A 1.544 MHz clock input used to generate internal clocks. Upon Loss of Signal (LOS), RCLK is derived from MCLK. If MCLK is not applied, this pin should be grounded.
TCLK	2	I	Transmit Clock	Transmit clock input. TPOS and TNEG are sampled on the falling edge of TCLK.
TPOS/ TDATA	3	I	Transmit Data Input	Input for data to be transmitted on the twisted-pair line. Normally, pin 3 is TPOS and pin 4 is TNEG, the positive and negative sides of a bipolar input pair. However, when pin 4 is held high for at least 16 TCLK cycles (equivalent to 15 successive bipolar violations), the 29C310/311 switches to a unipolar mode. Unipolar mode pin functions are listed in Table 2.
TNEG/ UBS	4	I	Data Input/ Polarity Select	
MODE	5	I	Mode Select	Setting MODE to logic 1 puts the 29C310 in the Host mode. In the Host mode, the serial interface is used to control the 29C310 and determine its status. Setting MODE to logic 0 puts the 29C310 in the Hardware (H/W) mode. In the Hardware mode the serial interface is disabled and hard-wired pins are used to control configuration and report status. Tying MODE to RCLK activates the Hardware mode and enables the B8ZS encoder/decoder.
RNEG/ BPV	6	O	Receive Negative Data	Bipolar data outputs. A signal on RNEG corresponds to receipt of a negative pulse on RTIP/RRING. A signal on RPOS corresponds to receipt of a positive pulse on RTIP/RRING. RNEG/RPOS outputs are Non-Return-to-Zero (NRZ). In Host mode, CLKE determines the clock edge at which these outputs are stable and valid. In Hardware mode both outputs are stable and valid on the rising edge of RCLK. In Unipolar mode, pin 6 output is a Bipolar Violation indication and pin 7 is the unipolar data output. See Table 2 for Unipolar mode functions.
RPOS/ RDATA	7	O	Receive Positive Data	
RCLK	8	O	Receive Clock	This is the clock recovered from the signal received at RTIP and RRING.
XTALIN	9	I	Crystal Input	An external crystal (18.7 pF load capacitance, pullable) operating at four times the bit rate (6.176 Mhz) is required to enable the jitter attenuation function of the 29C310. These pins may also be used to disable the jitter attenuator by connecting the XTALIN pin to the positive supply through a resistor, and tying the XTALOUT pin to ground.
XTALOUT	10	O	Crystal Output	
JASEL	11	I	Jitter Attenuation Select	Selects jitter attenuation location. When JASEL = 1, the jitter attenuator is active in the receive path. When JASEL = 0, the jitter attenuator is active in the transmit path.
LOS	12	O	Loss Of Signal	LOS goes to a logic 1 when 175 consecutive spaces have been detected. LOS returns to a logic 0 when the received signal reaches a mark density of 12.5 % (determined by receipt of four marks within 32 bit periods.) Received marks are output on RPOS and RNEG even when LOS is at logic 1.
TTIP	13	O	Transmit Tip	Differential Driver Outputs. These outputs are designed to drive a 50 -200 Ω load. Line matching resistors and transformer can be selected to give the desired pulse height.
TRING	16	O	Transmit Ring	
TGND	14	-	Tx Ground	Ground return for the transmit drivers power supply TV+.
TV+	15	I	Transmit Power Supply	+ 5 VDC power supply input for the transmit drivers. TV+ must not vary from RV+ by more than ± 0.3 V.

Table 1 : Pin Description (continued)

Symbol	Pin #	I/O	Name	Description
EGL	17	I	Equalizer Gain Limit	Input sets equalizer gain. When EGL = 0, up to 36 dB of equalizer gain may be added. When EGL = 1, equalizer gain is limited to no more than 26 dB.
LATN	18	O	Line Attenuation Indication (See Figure 8)	Encoded output. Pulse width, relative to RCLK, indicates receive equalizer gain setting (line insertion loss at 772 kHz) in 7.5 dB steps. When LATN = 1 RCLK pulse, the equalizer is set at 7.5 dB gain, 2 pulses = 15 dB, 3 pulses = 22.5 dB and 4 pulses = 0 dB. Output is valid on the rising edge of RCLK.
RTIP	19	I	Receive Tip	The AMI signal received from the line is applied at these pins. A 1:1 transformer is required. Data and clock from the signal applied at these pins are recovered and output on the RPOS/RNEG, and RCLK pins.
RRING	20	I	Receive Ring	
RV+	21	I	Receive Power Supply	+ 5 VDC power supply for all circuits except the transmit drivers. (Transmit drivers are supplied by TV+.)
RGND	22	-	Rx Ground	Ground return for power supply RV+.
NLOOP	23	O	Network Loopback (*H/W Mode*)	When high, indicates Inband Network Loopback has been activated by reception of 00001 pattern for five seconds. NLOOP is reset by reception of 001 for five seconds, or by activation of RLOOP or LLOOP.
$\overline{\text{INT}}$	23	O	Interrupt (*Host Mode*)	This 29C310 Host mode outgut goes low to flag the host processor when LOS or NLOOP changes state. $\overline{\text{INT}}$ is an open drain output and should be tied to power supply RV+ through a resistor. $\overline{\text{INT}}$ is reset by clearing the LOS or NLOOP register bit.
SDI	24	I	Serial Data In *(Host Mode)*	The serial data input stream is applied to this pin when the 29C310 operates in the Host mode. SDI is sampled on the rising edge of SCLK.
LBO1		I	Line Build-Out Select 1 (*H/W Mode*)	The signal applied at this pin in the 29C310 Hardware mode is used in conjunction with LBO2 to select the transmit line build-outs : 00 = 0 dB, 01 = 7.5 dB, 10 = 15 dB, and 11 = 22.5 dB.
SDO	25	O	Serial Data Out (*Host Mode*)	The serial data from the on-chip register is output on this pin in the 29C310 Host mode. If CLKE is high, SDO is valid on the rising edge of SCLK. If CLKE is low SDO is valid on the falling edge of SCLK. This pin goes to a high-impedance state when the serial port is being written to and when $\overline{\text{CS}}$ is high.
LBO2		I	Line Build-Out Select 2 (*H/W Mode*)	The signal applied at this pin in the 310 Hardware mode is used in conjunction with LBO1 to select the transmit line build-outs. 00 = 0 dB, 01 = 7.5 dB, 10 = 15 dB, and 11 = 22.5 dB.
$\overline{\text{CS}}$	26	I	Chip select *(Host Mode)*	This input is used to access the serial interface in the 29C310 Host mode. For each read or write operation, $\overline{\text{CS}}$ must transition from high to low, and remain low.
RLOOP		I	Remote Loopback (*H/W Mode*)	This input controls loopback in the 29C310 Hardware mode. Setting RLOOP to a logic 1 enables Remote Loopback. During Remote Loopback, in-line encoders and decoders are bypassed. Setting both RLOOP and LLOOP while holding TAOS low causes a Reset. Setting both RLOOP and LLOOP with TAOS high enables Network Loopback detect.

Table 1 : Pin Description (continued) (continued)

Symbol	Pin #	I/O	Name	Description
SCLK	27	I	Serial Clock *(Host Mode)*	This clock is used in the 29C310 Host mode to write data to or read data from the serial interface registers.
LLOOP		I	Local Loopback (*H/W Mode*)	This input controls loopback functions in the 29C310 Hardware mode setting LLOOP to a logic 1 enables the Local Loopback Mode. Setting both LLOOP and RLOOP while holding TAOS low causes a Reset.
CLKE	28	I	Clock Edge *(Host Mode)*	Setting CLKE to logic 1 causes RPOS and RNEG to be valid on the falling edge of RCLK, and SDO to be valid on the rising edge of SCLK. When CLKE is a logic 0, RPOS and RNEG are valid on the rising edge of RCLK, and SDO is valid on the falling edge of SCLK.
TAOS		I	Transmit All Ones (*H/W Mode*)	When set to a logic 1, TAOS causes the 29C310 (Hardware mode) to transmit a continuous stream of marks at the TCLK frequency. Activating TAOS causes TPOS and TNEG inputs to be ignored. TAOS is inhibited during Remote Loopback. Setting TAOS, LLOOP and RLOOP simultaneously enables Network Loopback.

Functional Description

The 29C310 is fully integrated PCM transceiver for 1.544 MHz (T1) applications. It allows full-duplex transmission of digital data over existing twisted-pair installations.

The 29C310 transceiver interfaces with two twisted-pair lines (one twisted-pair for transmit, one twisted-pair for receive) through standard pulse transformers and appropriate resistors.

Figure 1 is a block diagram of the 29C310. This transceiver may be controlled by a microprocessor through the serial port (Host Mode), or by individual pin settings (Hardware Mode). The jitter attenuator may be positioned in either the transmit or receive path.

Table 2 : Unipolar Data I/O Pin Description

Symbol	Pin #	I/O	Name	Description
TDATA	3	I	Transmit Data Input	Unipolar input for data to be transmitted on the twisted-pair line.
UBS	4	I	Uni-Bi Polarity Select	When pin 4 is held high for at least 16 TCLK cycles (equivalent to 15 successive bipolar violations), the 29C310 switches to unipolar data I/O. The device immediately returns to bipolar I/O when pin 4 goes low.
BPV	6	O	Bipolar Violation	Pin 6 goes high when a bipolar violation is received.
RDATA	7	O	Receive Data	Unipolar data output. RDATA is a Non-Return-to-Zero (NRZ) output. In Host mode, CLKE determines the clock edge at which RDATA is stable and valid. In Hardware mode RDATA is stable and valid on the rising edge of RCLK.
Note : Table 2 lists only those pins which are affected by the switch to unipolar data I/O.				

Transmitter

The transmitter circuits in the 29C310 are identical. Input data (bipolar or unipolar) for transmission onto the line is clocked serially into the device. Bipolar data input at pin 3 (TPOS) and pin 4 (TNEG). Unipolar data is input at pin 3 (TDATA) only. (Unipolar mode is enabled by holding pin 4 high for 16 RCLK cycles). Input data may be passed through the Jitter Attenuator and/or B8ZS encoder, if selected. In Host mode, B8ZS is selected by setting bit D3 of the input data byte. In Hardware mode, B8ZS is selected by connecting the MODE pin to RCLK. Input synchronization is supplied by the transmit clock (TCLK). Timing requirements for TCLK and the Master Clock (MCLK) are defined in Table 3 and Figure 3.

Idle Mode

The 29C310 incorporates a transmit idle mode. This allows multiple transceivers to be connected a single line for redundant applications. TTIP and TRING remain in a high impedance state when TCLK is not present (TCLK grounded). The high impedance state can be temporarily disabled by enabling one of the diagnostic modes : Remote Loopback, Local Loopback or Network Loopback.

The transmitted pulse shape is determined by Line Build Out (LBO) inputs LBO1 and LBO2 as follows :

Line Build-Out (dB)	Ω	7.5	15	22.5
LBO1	0	1	0	1
LBO1	0	0	1	1

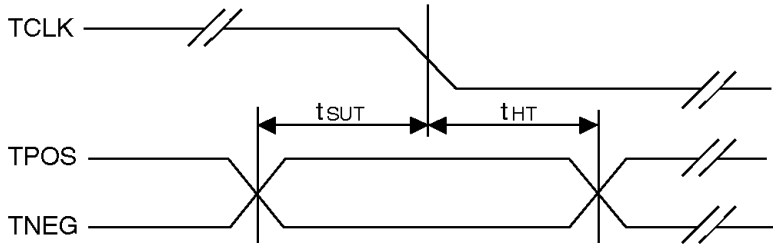
LBO settings are input through the serial port in the 29C310 Host mode. In the Hardware mode, LBO inputs are applied through individual pins. Shaped pulses meeting the various T1 CSU and ISDN PRI requirements are applied to the AMI line driver for transmission onto the line at TTIP and TRING. Refer to Table 4 and Figure 4 for T1 pulse mask specifications.

Table 3 : 29C310 Master Clock and Transmit Timing Characteristics (See Figure 3)

Symbol	Parameter	Min	Typ[1]	Max	Units	Notes
MCLK	Master clock frequency	-	1.544	-	MHz	
MCLKt	Master clock tolerance	-	± 100	-	ppm	
MCLKd	Master clock duty cycle	40	-	60	%	
fc	Crystal frequency	-	6.176	-	MHz	
TCLK	Transmit clock frequency	-	1.544	-	MHz	
TCLKt	Transmit clock tolerance	-	-	± 100	ppm	
TCLKd	Transmit clock duty cycle	10	-	90	%	
t_{SUT}	TPOS/TNEG to TCLK setup time	50	-	-	ns	
t_{HT}	TCLK to TPOS/TNEG Hold time	50	-	-	ns	

Note : 1. Typical figures are at 25 °C and are for design aid only ; not guaranteed and not subject to production testing.

Figure 3. 29C310 Transmit Clock Timing



Short Circuit Limit

The 29C310 transmitter is equipped with a short-circuit limiter. This feature limits to approximately 60 mA RMS the current the transmitter will source into a low-impedance load. The limiter trips when the RMS current exceeds the limit for 100 µs (~150 marks). It automatically resets when the load current drops below the limit.

The 29C310 matches FCC and AT&T specifications for CSU and NI applications, as well as ANSI T1E1, and CCITT requirements for ISDN PRL.

Line Code

The 29C310 transmits data as a 50 % AMI line code as shown in Figure 5. Power consumption is reduced by activating the AMI line driver only to transmit a mark. The output driver is disabled during transmission of a space. Biasing of the transmit DC level is on-chip.

Receiver

The twisted-pair input is received via a 1:1 transformer. Recovered data is output at RPOS/RNEG (RDATA in unipolar mode), and the recovered clock is output at RCLK. Refer to Table 5 and Figure 6 for receiver timing.

Figure 4. 1.544 MHz T1 Pulse Mask.

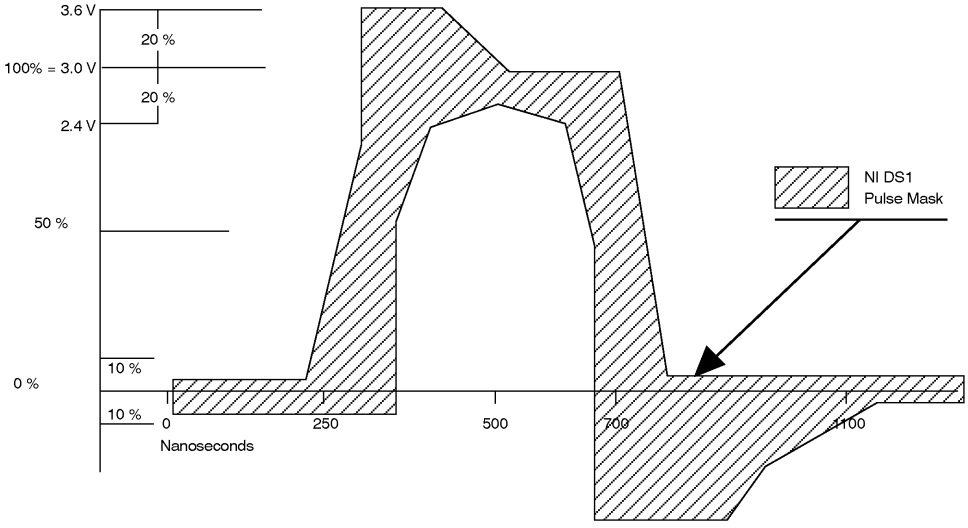
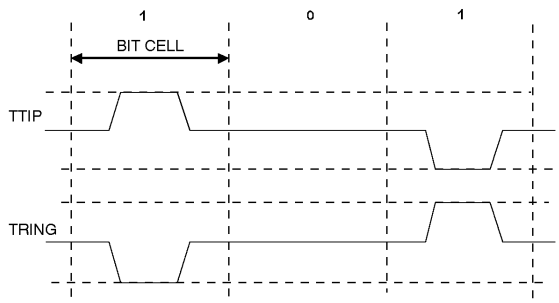


Table 4 : Pulse Mask Corner Point Specifications.

Maximum Curve		Minimum Curve	
Time (ns)	**% V**	**Time (ns)**	**% V**
0	5	0	-5
250	5	350	-5
325	80	350	50
325	120	400	90
425	120	500	95
500	105	600	90
675	105	650	50
725	5	650	-45
1100	5	800	-45
1250	5	896	-26
		1100	-5
		1250	-5

Figure 5. 50 % Ami Coding Diagram.



The signal received at RPOS and RNEG is processed through the receive equalizer. The Equalizer Gain Limit (EGL) input determines the maximum gain that may be applied at the equalizer. When set to 0, up to 36 dB of gain may be applied.

When EGL = 1, gain is limited to no more than 26 dB providing fro increased noise margin in shorter loop operation. Insertion loss of the line in 7.5 dB steps, as indicated by the receive equalizer setting, is encoded in the LATN output as shown in Figure 7.

Table 5 : 29C310 Receive Timing Characteristics (See Figure 6).

Symbol	Parameter	Min	Typ[1]	Max	Units
RCLKd	Receive clock duty cycle[2]	40	50	60	%
t_{PW}	Receive clock pulse width[2]	600	648	700	ns
t_{PWH}	Receive clock pulse width high	-	324	-	ns
t_{PWL}	Receive clock pulse width low	303	324	345	ns
t_{SUR}	RPOS/RNEG to RCLK rising setup time	-	274	-	ns
t_{HR}	RCLK rising to RPOS/RNEG hold time	-	274	-	ns

Notes : 1. Typical figures are at 25 °C and are for design aid only ; not guaranteed and not subject to production testing.
2. RCLK duty cycle widths will vary depending on extent of received pulse jitter displacement. Max and Min RCLK duty cycles are for worst case jitter conditions (0.4 UI clock displacement for 1.544 MHz).

Figure 6. 29C310 Receive Clock Timing

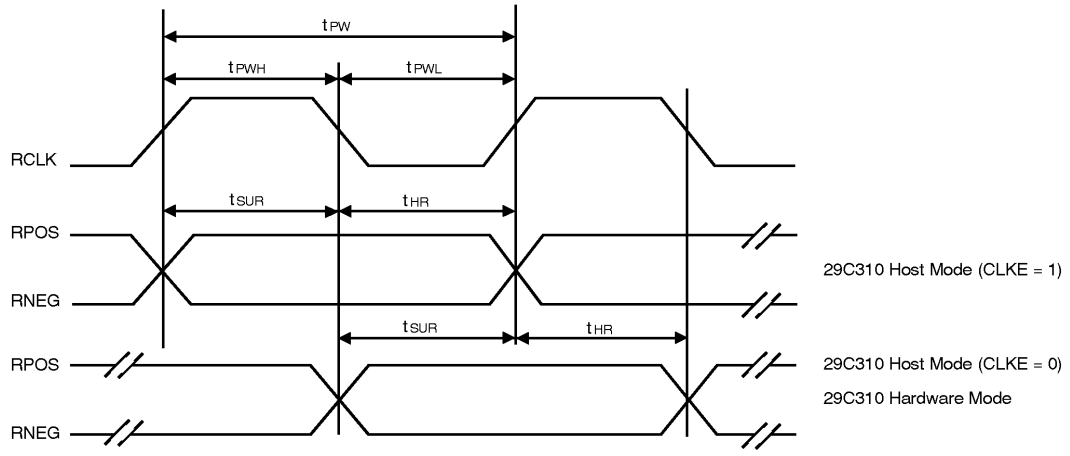
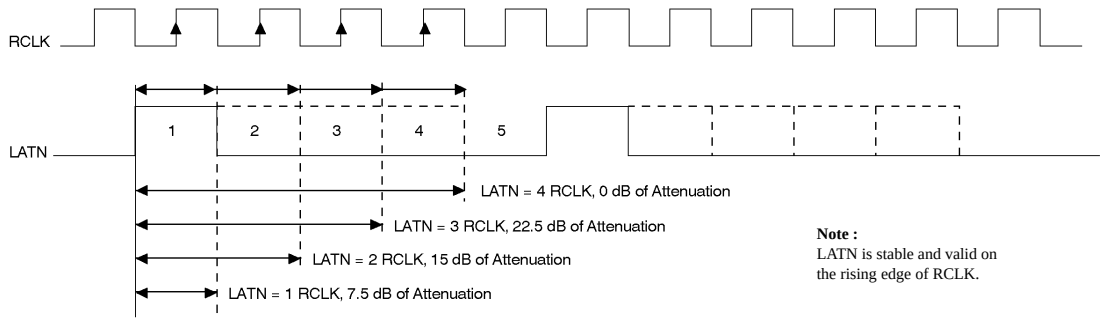


Figure 7. LATN Pulse Width Encoding



The equalized signal is filtered and applied to the peak detector and data slicers. The peak detector samples the inputs and determines the maximum value of the received signal. A percentage of the peak value is provided of the data slicers as a threshold level to ensure optimum signal-to-noise ratio. The threshold is set to 50 % of the peak value. The receiver is capable of accurately recovering signals with up to 36 dB of cable attenuation (from 2.4 V).

After processing through the data slicers, the received signal is routed to the data and timing recovery section, then to the B8ZS decoder (if selected) and to the LOS processor. The LOS Processor loads a digital counter at the RCLK frequency. The count is incremented each time a zero (space) is received, and reset to zero each time a one (mark) is received. Upon receipt of 175 consecutive zeros the LOS pin goes high, and a smooth transition replaces the RCLK output with the MCLK. (*During LOS in the 29C310, if MCLK is not supplied and JASEL = 1, the RCLK output is replaced with the centered crystal clock.)*

Received marks will be output regardless of the LOS status, but the LOS pin will not reset until the ones density reaches 12,5 %. This level is based on receipt of at least 4 ones in any 32 bit periods.

Jitter Attenuation

Jitter attenuation, available in the 29C310 is provided by a Jitter Attenuation Loop (JAL) and an Elastic Store (ES). An external crystal oscillating at 4 times the bit rate provides clock stabilization. Refer to Table 6 for crystal specifications. The ES is a 32 × 2-bit register. When JASEL = 1, the JAL is positioned in the receive path. When JASEL = 0, the JAL is positioned in the transmit path.

Data (TPOS/TNEG/TDATA or RPOS / RNEG / RDATA) is clocked into the ES with the associated clock signal (TCLK or RCLK), and clocked out of the ES with the dejittered clock from the JAL. When the bit count in the ES is within two bits of overflowing or underflowing, the ES adjusts an average delay of 16 bits in the associated path.

Operating Modes

The 29C310 can be controlled by a microprocessor through a serial interface (Host Mode), or through individual pins, (Hardware mode). The mode of operation is set by the MODE pin logic level.

Table 6 : Crystal Specifications (External).

Parameter	Specification
Frequency	6.176 MHz
Frequency Stability	± 20 ppm @ 25°C ± 25 ppm from -40 °C to + 85 °C (Ref 25 °C reading)
Pullability	CL = 11 pF to 18.7 pF, +ΔF = 175 to 195 ppm CL = 18.7 pF to 34 pF, -ΔF = 175 to 195 ppm
Effective series resistance	40 Ω Maximum
Crystal cut	AT
Resonance	Parallel
Maximum drive level	2.0 mW
Mode of operation	Fundamental
Crystal holder	HC49 (R3W), C_o = 7 pF maximum C_M = 17 fF typical

Host Mode Operation

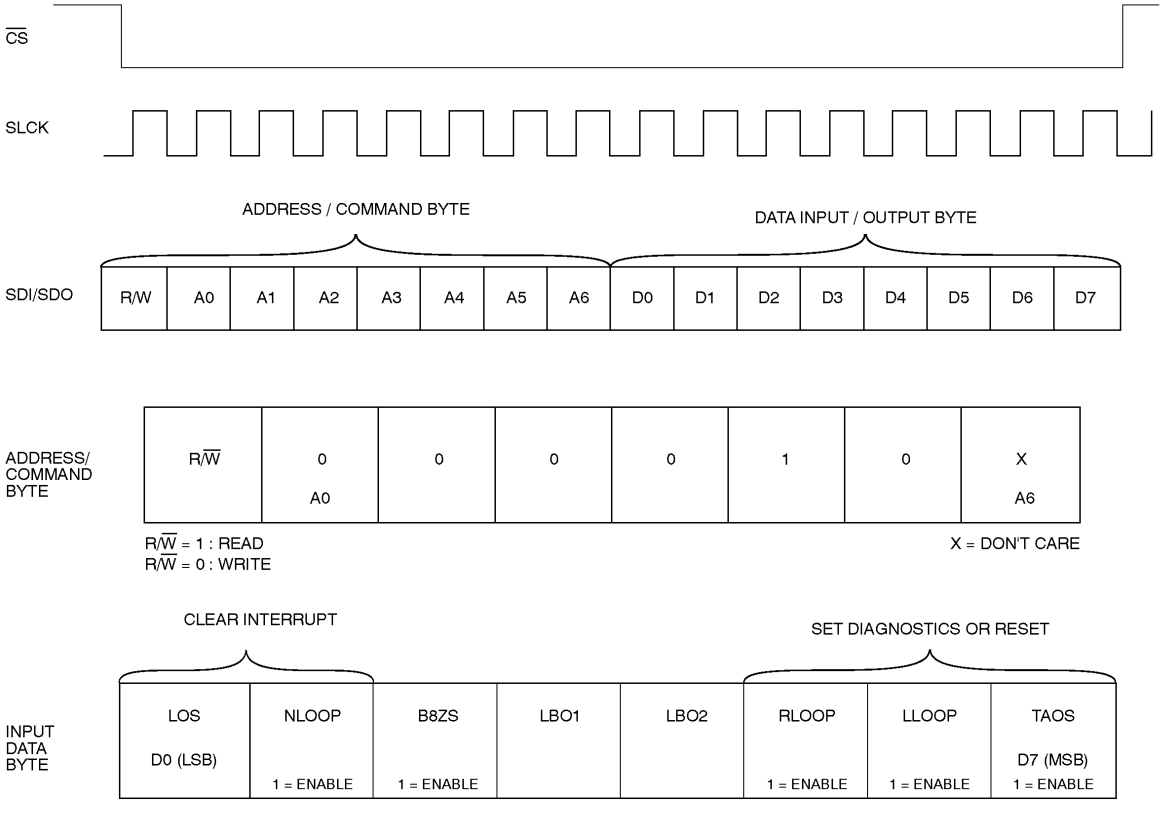
The 29C310 operates in the Host mode when MODE is set to 1. The 16-bit serial consists of an 8-bit Command/Address byte and an 8-bit Data byte. Table 7 lists the output data bit combinations. Figure 8 shows the serial interface data structure and timing. The Host mode provides a latched Interrupt output (INT) which is triggered by a change in the LOS or NLOOP bits. The Interrupt is cleared when the interrupt condition no longer exists, and the host processor writes a one to the respective bit in the serial input data byte. Host most also

allows control of the serial data and receive data output timing. The Clock Edge (CLKE) signal determines when the outputs are valid, relative to the Serial Clock (SCLK) or RCLK as listed in Table 8.

Table 7 : 29C310 Serial Data Output Bit Coding (See Figure 8).

BIT D5	BIT D6	BIT D7	Status
0	0	0	Reset has occurred, or no program input
0	0	1	TAOS active
0	1	0	LLOOP active
0	1	1	TAOS and LLOOP active
1	0	0	RLOOP active
1	0	1	NLOOP has changed state since last Clear NLOOP occurred
1	1	0	LOS has changed state since last Clear LOS occurred
1	1	1	LOS and NLOOP have both changed state since last Clear NLOOP and Clear LOS occurred

Figure 8. 29C310 Serial Interface Data Structure



Note : Output Data Byte same as Input Data Byte shown above, except for Bits D5 through D7 listed in Table 7.

Table 8 : CLKE Settings.

CLKE	Output	Clock	Valid Edge
LOW	RPOS	RCLK	Rising
	RNEG	RCLK	Rising
	SDO	SCLK	Falling
HIGH	RPOS	RCLK	Falling
	RNEG	RCLK	Falling
	SDO	SCLK	Rising

The 29C310 serial port is addressed by setting bit A4 in the Address/Command byte, corresponding to address 16. The 29C310 contains only a single output data register so no complex chip addressing scheme is required. The register is accessed by causing the Chip Select (CS) input to transition from high to low. Bit 1 of the serial Address/Command byte provides Read/Write control when the chip is accessed. A logic 1 indicates a read operation, and a logic 0 indicates a write operation. Serial data I/O timing characteristics are shown in Table 11, and figures 12 and 13, in the Electrical Characteristics section.

Hardware Mode Operation

In Hardware mode the transceiver is accessed and controlled through individual pins. With the exception of the INT and CLKE functions, Hardware mode provides all the functions provided in the Host mode. In the Hardware mode RPOS/RNEG or RDATA outputs are valid on the rising edge of RCLK. The 29C310 operates in Hardware mode only when MODE is set to 0 or connected to RCLK.

Initialization and Reset Operation

Upon power up, the transceiver is held static until the power supply reaches approximately 3 V. Upon crossing this threshold, the device begins a 32 ms reset cycle to calibrate the transmit and receive delay lines and lock the Phase Lock Loop to the receive line. A reference clock is required to calibrate the delay lines. The transmitter reference is provided by TCLK.

The crystal oscillator provides the receiver reference in the 29C310. If the 29C310 crystal oscillator is grounded, MCLK is used as the receiver reference clock.

The transceiver can also be reset from the Host or Hardware mode. In Host mode, reset is commanded by simultaneously writing ones to RLOOP and LLOOP, and a zero to TAOS. In Hardware mode, reset is commanded by holding RLOOP and LLOOP high simultaneously for 200 ns while holding TAOS low. In either mode, reset clears and set all registers to 0.

Diagnostic Mode Operation

In Transmit All Ones (TAOS) mode the TPOS and TNEG inputs to the transceiver are ignored and the transceiver transmits a continuous stream of 1’s at the TCLK frequency. (In the 29C310 with JASEL = 0 and TCLK not provided, TAOS is locked to the MCLK.) This can be used as the Blue Alarm Indicator (AIS). In Host mode, TAOS is commanded by writing a one to bit D7 of the input data byte. In Hardware mode, TAOS is commanded by setting pin 28 high. TAOS can be commanded simultaneously with Local Loopback, but is inhibited during Remote Loopback.

Local Loopback (LLOOP) is designed to exercize the maximum number of functional blocks. During LLOOP operation, the RTIP/RRING inputs from the line are disconnected. Instead, the transmit outputs are routed back into the receive inputs. This tests the encoders/decoders, jitter attenuator, transmitter, receiver and timing recovery sections. In Host mode, Local Loopback is commanded by writing a one to bit D6 of the input data byte. In Hardware mode, Local Loopback is commanded by setting pin 27 high.

In Remote Loopback (RLOOP) mode, the transmit data and clock inputs (TCLK and TPOS/TNEG or TDATA) are ignored, and the in-line encoders and decoders are bypassed. The RPOS/RNEG or RDATA outputs are looped back through the transmit circuits and output on TTIP and TRING at the RCLK frequency. Receiver circuits are unaffected by the RLOOP command and continue to output the RCLK and RPOS/RNEG or RDATA signals received from the twisted-pair line. In Host mode, Remote Loopback is commanded by writing a one to bit D5 of the input data byte. In Hardware mode, Remote Loopback is commanded by setting pin 26 high.

Network Loopback can be commanded from the network when the Network Loopback detect function is enabled. In Host mode, Network Loopback (NLOOP) detection is enabled by simultaneously writing ones to RLOOP, LLOOP and TAOS. In Hardware mode, Network Loopback detection is enabled by holding RLOOP, LLOOP and TAOS high simultaneously for 200 ns. NLOOP detection may be disabled by resetting the chip.

When NLOOP detection is enabled, the receiver monitors the input data stream for the NLOOP data patterns (00001 = enable, 001 = disable). When an NLOOP enable data pattern is repeated for a minimum of five seconds (with 10^{-3} BER), the device begins remote loopback operation. The 29C310 responds to both framed and unframed NLOOP patterns. Once remote network

loopback detection is enabled at the chip and activated by the correct data pattern, it is identical to remote loopback initiated at the chip. NLOOP is reset by receiving the disable pattern for 5 seconds, or by activation of either RLOOP or LLOOP.

Application Considerations

LATN Decoding Circuits And External Components

To conserve pins, the line attenuation output is encoded as a simple serial bit stream. Table 9 provides the decoded output for each equalizer setting. Figure 10 is a typical decoding circuit for the LATN output. It uses a 2-bit synchronous counter (half of a 4-bit counter) with synchronous reset, and a pair of flip-flops. Table 10 lists approved crystals and transformers.

Power Requirements

The 29C310 is low-power CMOS device. It operates from a single +5 V power supply which can be connected externally to both the transmitter and receiver. However, the two inputs must be within ± 3 V of each other, and decoupled to their respective grounds separately, as shown in Figure 9. Isolation between the transmit and receive circuits is provided internally.

Table 9 : LATN Output Coding.

L1	L2	LINE ATTENUATION
0	0	0.0 dB
0	1	-7.5 dB
1	0	-15.0 dB
1	1	-22.5 dB

Figure 9. Typical LATN Decoding Circuit.

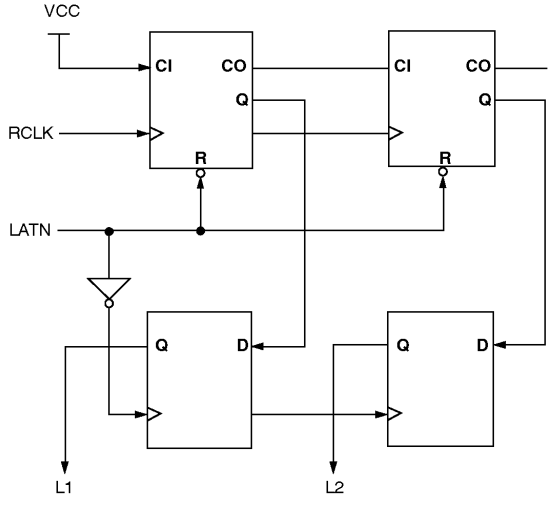


Table 10 : Approved Crystals and Transformers.

Component	Manufacturer	Part Numbers
Crystal	M-Tron Monitor Products CTS Knights Valpey Fisher U.S. Crystal	MP-1 MSC1311-01B 6176-180 VF49A16FN1 U18-18-6176SP
Tx Transformer	Pulse Engineering Bell Fuse Midcom Schott Corp	64931 and 65351 0553-5006-IC 671-5832 67112060 and 67115100
Rx Transformer	Schott Corp Pulse Engineering	67109510 64936 and 65400

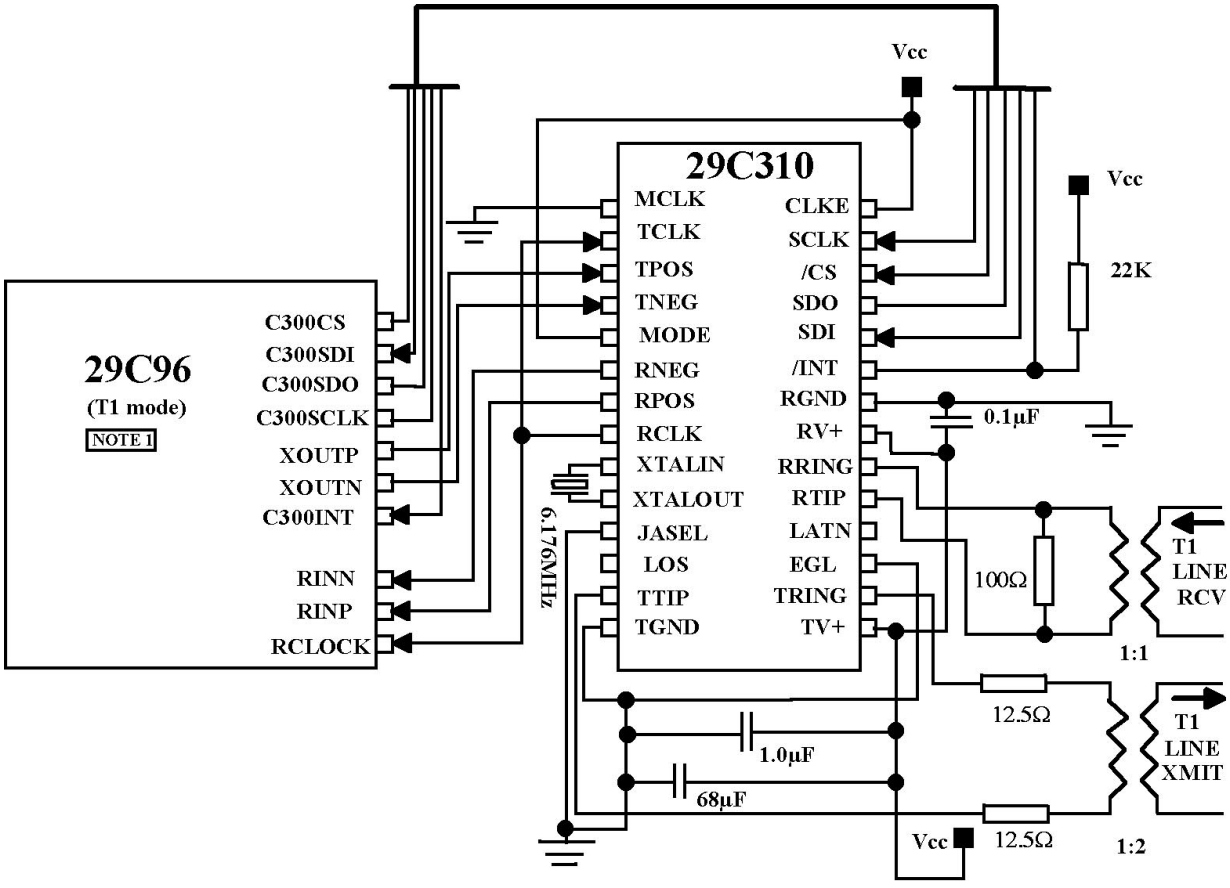
T1 CSU Interface Applications Host Mode

Figure 10 shows a typical T1 CSU application with the 29C310 operating in the Host mode (MODE pin tied high). The 29C96 T1/ESF Framer provides the digital interface with the host controller. The device is controlled through the serial interface. In the Host mode, the LOS alarm is reported via the serial port so the LOS pin is allowed to float.

A Clock Adapter (CLAD) provides the 2.048 MHz system backplane clock, locked to the recovered 1.544 MHz clock signal. The 6.176 MHz crystal across XTALIN and XTALOUT enables the JAL which is switched to the transmit side by the ground on JASEL. (Refer to Table 10 for approved crystals and transformers.) The power supply inputs are tied to a common bus with appropriate decoupling capacitors (68 µF and 0.1 µF) installed on each side.

The twisted-pair interfaces are relatively simple. A 100 Ω resistor across the input of a 1:1 transformer is used on the receive side, and a pair of 12.5 Ω resistors are installed in line with the 1:2 output transformer.

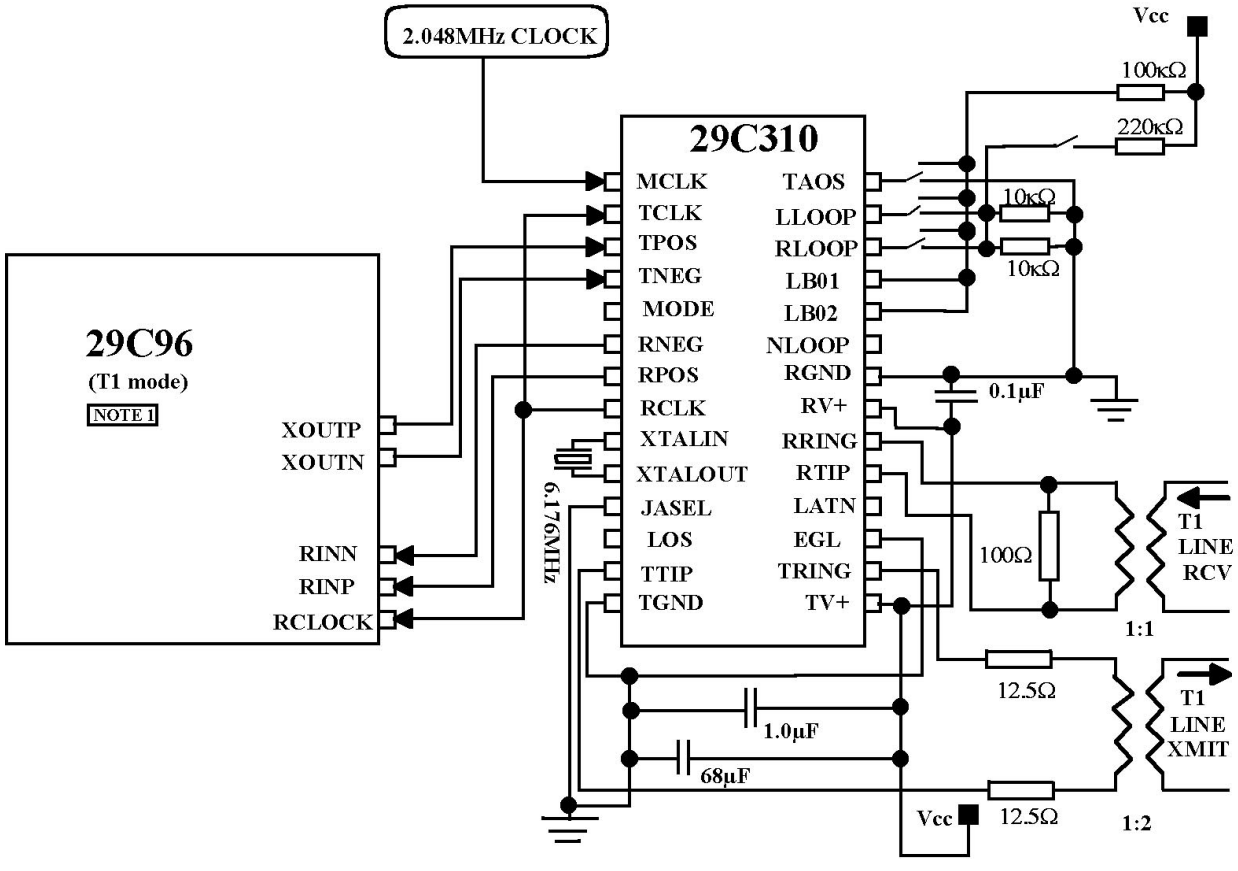
Figure 10. Typical 29C310 Host Mode T1/CSU Application



Hardware Mode Applications

Figure 11 is a typical 1.544 MHz ISDN PRI application with the 29C310 operating in the Hardware mode (pin 5 grounded) with the 29C96 Framer. As in the T1 CSU application Figure 10, this configuration is illustrated with a single power supply bus. Both LBO pins are set high, selecting the 22.5 dB LBO, and the EGL pin is grounded allowing for full receiver gain. The hard-wired control lines for TAOS, LLOOP and RLOOP diagnostic modes are individually controllable. The LLOOP and RLOOP lines are also tied to a single control for the Reset function. The receive and trasmit line interfaces are identical to the Host mode application shown in Figure 10.

Figure 11. Typical 29C310 Hardware Mode Application.



Electrical Characteristics

Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units
RV+, TV+	DC supply (referenced to GND)	-	6.0	V
V_{IN}	Input voltage, any pin	RGND -0.3	RV+ + 0.3	V
I_{IN}	Input current, any pin[1]	-10	10	mA
T_A	Ambient operating temperature	-40	85	°C
T_{STG}	Storage temperature	-65	150	°C

WARNING : Operations at or beyong these limits may result in permanent damages to the device. Normal operation not guaranteed at these extremes.

Note : 1. Transient currents of up to 100 mA will not cause SCR latch-up. TTIP, TRING, TV+ and TGND can withstand a continuous current of 100 mA.

Operating Conditions/Characteristics

Symbol	Parameter	Min	Typ [1]	Max	Units	Test Conditions
RV+, TV+	DC supply[2]	4.75	5.0	5.25	V	
T_A	Ambient operating temperature	-	25	-	°C	
P_D	Power dissipation[3]	-	300	-	mW	100 % ones density & maximum line length @ 5.25 V

Notes : 1. Typical figures are at 25 °C and are for design aid only ; not guaranteed and not subject to production testing.
2. TV+ must not exceed RV+ by more than 0.3 V.
3. Power dissipation while drivings 25 Ω load over operating temperature range. Includes device and load. Digital input levels are within 10 % of the supply rails and digital outputs are driving a 50 pF capacitive load.

Digital Characteristics (T_A = -40° to 85°C, V+ = 5.0 V ± 5 %, GND = 0 V)

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
V_{IH}	High level input voltage [1,2] (pins 1-5, 10, 23-28)	2.0	-	-	V	
V_{IL}	Low level input voltage [1,2] (pins 1-5, 10, 23-28)	-	-	0.8	V	
V_{OH}	High level output voltage [1,2] (pins 6-8, 10, 23-25)	2.4	-	-	V	I_{OUT} = -400 µA
V_{OL}	Low level output voltage [1,2] (pins 6-8, 10, 23-25)	-	-	0.4	V	I_{OUT} = 1.6 mA
I_{LL}	Input leakage current	0	-	± 10	µA	
I_{IL}	Three-state leakage current[1] (pin 25)	0	-	± 10	µA	

Notes : 1. Functionality of pins 23 and 25 depends on mode. See Host/Hardware Mode descriptions.
2. Output drivers will output CMOS logic levels into CMOS loads.

Analog Characteristics (T_A = -40° to 85°C, V+ = 5.0 V ± 5 %, GND = 0 V)

Parameter		Min	Typ[1]	Max	Units	Test conditions
Recommended output load at TTIP and TRING		50	-	200	Ω	
AMI Output Pulse Amplitudes		2.4	3.0	3.6	V	
Jitter added by the transmitter[2]	10 Hz -8 kHz[3]	-	-	0.005	UI	measured at the output with LBO1 = 0, and LBO2 = 0
	8 kHz -40 kHz[3]	-	-	0.01	UI	
	10 Hz -40 kHz[3]	-	-	0.01	UI	
	Broad Band	-	-	0.04	UI	LBO2 = 0
Receive signal attenuation	Mode 1 (EGL = 1)	0	26	-	dB	
range @ 772 kHz	Mode 2 (EGL = 0)	0	36	-	dB	
Allowable consecutive zeros before LOS		160	175	190	-	
Input jitter tolerance	10 kHz -100 kHz	0.4	-	-	UI	0 -26 dB
		0.3	-	-	UI	26 -36 dB
	1 Hz	138	-	-	UI	
Jitter attenuation curve corner frequency[4]		-	6	-	Hz	

Notes : 1. Typical figures are at 25 °C and are for design aid only ; not guaranteed and not subject to production testing.
2. Input signal to TCLK is jitter-free.
3. Guaranteed by characterization ; not subject to productions testing.
4. Circuit attenuates jitter at 20 dB/decade above the corner frequency.

Table 11 : 29C310 Serial I/O Timing Characteristics (See Figures 12 and 13).

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Rise/Fall time -any digital output	t_{RF}	-	-	100	ns	Load 1.6 mA, 50 pF
SDI to SCLK setup time	t_{DC}	50	-	-	ns	
SCLK to SDI hold time	t_{CDH}	50	-	-	ns	
SCLK low time	t_{CL}	240	-	-	ns	
SCLK high time	t_{CH}	240	-	-	ns	
SCLK rise and fall time	t_R, t_F	-	-	50	ns	
CS to SCLK setup time	t_{CC}	50	-	-	ns	
SCLK to CS hold time	t_{CCH}	50	-	-	ns	
CS inactive time	t_{CWH}	250	-	-	ns	
SCLK to SDO valid	t_{CDV}	-	-	200	ns	
SCLK falling edge or CS rising edge to SDO high Z	t_{CDZ}	-	100	-	ns	
Note : 1. Typical figures are at 25 °C and are for design aid only ; not guaranteed and not subject to production testing						

Figure 12. 29C310 Serial Data Input Timing Diagram

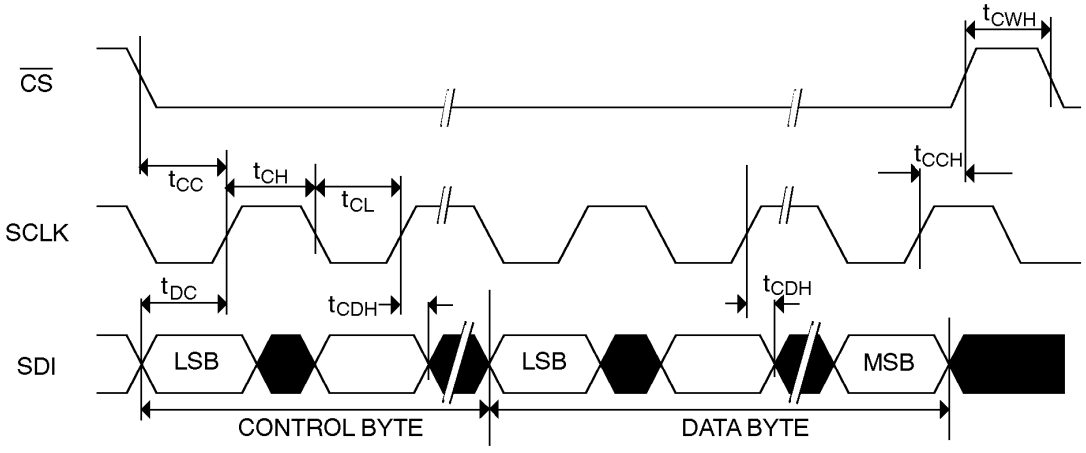
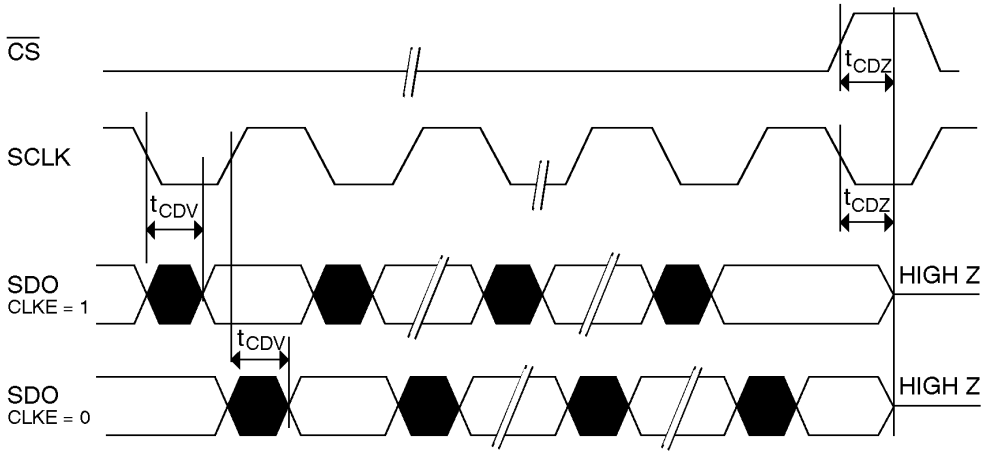


Figure 13. 29C310 Serial Data Output Timing Diagram



Ordering Information

∅ — Temperature Range
∅ Commercial
I Industrial

S — Packages :
S = PLCC
P = PDIL

29C3XX — Part Number
29C300
29C301
29C304
29C305
29C310
29C318

A — A = Low Power
- 29C304A
- 29C305A

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